Reg.No. _____

Karunya UNIVERSITY

(Karunya Institute of Technology & Sciences)
(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

End Semester Examination – Nov/Dec – 2016

Code : 14EC3020
Sub. Name : CMOS VLSI Design

Semester : 2016-17 ODD
Duration : 3hrs
Max. marks : 100

ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)

Q. No.	Sub Div.	Questions	Course Outcome	Marks
1.	a.	Calculate the threshold voltage V_{TO} at V_{SB} = 0, for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping density $N_A=10^{16}$ cm^{-3}, polysilicon gate doping density $N_D=2x10^{20}$ cm^{-3}, gate oxide thickness t_{ox}=500Å, and oxide interface fixed charge density $N_{ox} = 4x10^{10}cm^{-2}$.	CO1	**8**
	b.	With Gradual Channel Approximation (GCA) method find the derivation of I_D Cutoff, Non Saturation and Saturation region and draw the Drain voltage Vs Drain current characteristics.	CO1	**12**
		(OR)		
2.	a.	Examine the mechanisms of channel pinch-off and current flow in saturation mode and discuss about channel length modulation.	CO1	**8**
	b.	(a) Discuss in detail about the Oxide related and Junction capacitances.	CO1	**12**
3.	a.	Explain the DC and transfer characteristics of CMOS inverter and derive the expression for output voltage in various operating regions.	CO1	**12**
	b.	Synthesis a complex CMOS gate whose function is $F = D + A\cdot (B + C)$.	CO1	**8**
		(OR)		
4.	a.	Explain the concepts involved in Robust and Efficient Pass-Transistor Design.	CO3	**14**
	b.	Consider 16 cascaded minimum sized transmission gates, each with an average resistance of 8kΩ.The node capacitance consists of the capacitance of two NMOS and PMOS devices. The capacitance is 3.6fF.Find the propagation delay of a network of 16 transmission gates.	CO1	**6**
5.	a.	Explain about propagation delay of CMOS Gate and obtain the equivalent RC model for 2-input CMOS gate.	CO1	**8**
	b.	Explain in detail about the design techniques for large fan-in	CO1	**12**
		(OR)		
6.	a.	Explain in detail the various signal integrity issues in Dynamic CMOS logic.	CO3	**14**
	b.	Draw the function Z= A.B+ C.D using Domino CMOS Logic.	CO3	**6**

7.	a.	Define ratioed logic and explain in detail about pseudo NMOS logic.	CO3	**10**
	b.	With neat diagram explain in detail about DCVSL and pass transitor logic.	CO3	**10**
		(OR)		
8.	a.	Discuss in detail about cascading Dynamic CMOS logic.	CO3	**7**
	b.	Discuss in detail about Dynamic Transmission gate edge triggered and C^2MOS master slave positive edge triggered register.	CO3	**10**
	c.	Draw the basic block of np-CMOS logic.	CO3	**3**
		Compulsory:		
9.	a.	Draw the stick diagram and layout of 2-input CMOS NOR Gate	CO2	**5**
	b.	Draw the basic block of 4X4 array multiplier.	CO3	**5**
	c.	With neat diagram explain in detail about carry by pass adder and also design 16-bit carry by pass adder.	CO3	**10**

ALL THE BEST